

Dual N-channel MOSFET

KFCAB12004NL

Datasheet

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET for lithium-ion secondary battery protection circuits.

2. FEATURES

- Source-source On-state Resistance: $R_{SS(on)}$ typ = 3.2 m Ω (V_{GS} = 3.3 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

3. MARKING SYMBOL: R8

4. PACKAGING

Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

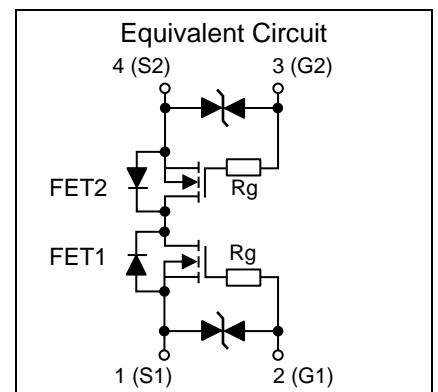
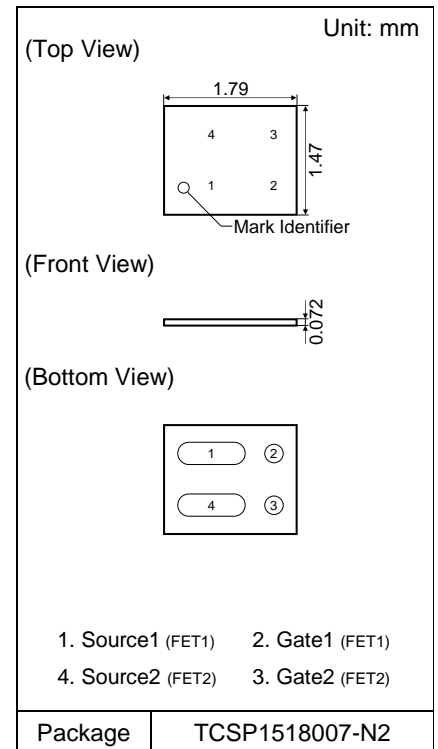
5. ABSOLUTE MAXIMUM RATINGS $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Rating | Unit |
|--|-----------|---------------|------------------|
| Source-source Voltage | VSS | 12 | V |
| Gate-source Voltage | VGS | ± 8 | V |
| Source Current | DC *1 | IS1 | A |
| | DC *2 | IS2 | |
| | DC *3 | IS3 | |
| | Pulsed *4 | ISp | |
| Total Power Dissipation | DC *1 | PD1 | W |
| | DC *2 | PD2 | |
| | DC *3 | PD3 | |
| Operating Junction and Storage Temperature Range | Tj, Tstg | - 55 to + 150 | $^\circ\text{C}$ |

6. THERMAL CHARACTERISTICS $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Rating | Unit |
|---------------------------|---------|--------|-----------------------------|
| Thermal Resistance (ch-a) | Rth1 *1 | 255 | $^\circ\text{C} / \text{W}$ |
| | Rth2 *2 | 89 | |
| | Rth3 *3 | 50 | |

- Note
- *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (23 mm² area, 36 μm thickness).
 - *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (604 mm² area, 36 μm thickness).
 - *3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
 - *4 $t = 10 \mu\text{s}$, Duty Cycle $\leq 1\%$.



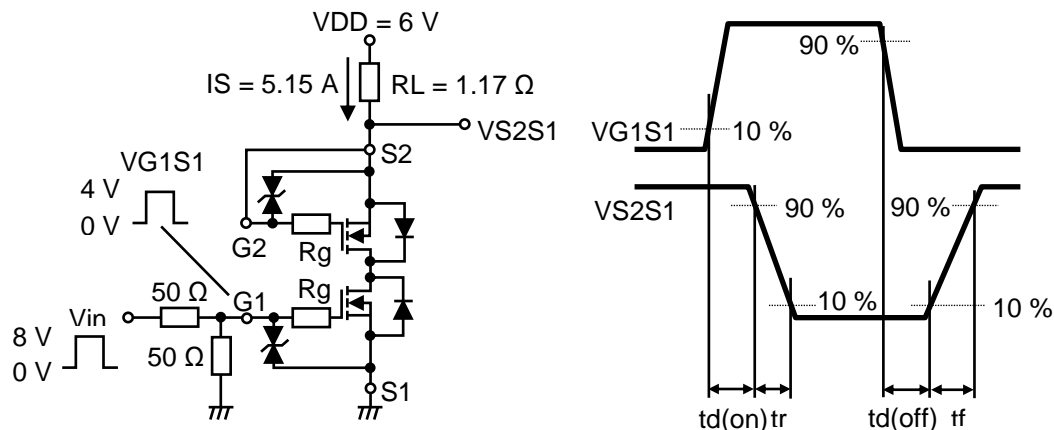
7. ELECTRICAL CHARACTERISTICS $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|--------------|---|------|------|-----------|------------------|
| Source-source Breakdown Voltage | VSSS | $I_S = 1\text{ mA}$, $V_{GS} = 0\text{ V}$ | 12 | | | V |
| Zero Gate Voltage Source Current | ISSS | $V_{SS} = 12\text{ V}$, $V_{GS} = 0\text{ V}$ | | | 1 | μA |
| Gate-source Leakage Current | IGSS1 | $V_{GS} = \pm 8\text{ V}$, $V_{SS} = 0\text{ V}$ | | | ± 5 | μA |
| | IGSS2 | $V_{GS} = \pm 5\text{ V}$, $V_{SS} = 0\text{ V}$ | | | ± 0.5 | |
| Gate-source Threshold Voltage | V_{th} | $I_S = 0.50\text{ mA}$, $V_{SS} = 6\text{ V}$ | 0.35 | 0.90 | 1.40 | V |
| Source-source On-state Resistance | RSS(on)1 | $I_S = 5.15\text{ A}$, $V_{GS} = 4.5\text{ V}$ | 1.95 | 2.90 | 3.70 | $\text{m}\Omega$ |
| | RSS(on)2 | $I_S = 5.15\text{ A}$, $V_{GS} = 3.8\text{ V}$ | 2.00 | 3.15 | 4.10 | |
| | RSS(on)3 | $I_S = 5.15\text{ A}$, $V_{GS} = 3.3\text{ V}$ | 2.05 | 3.20 | 4.55 | |
| | RSS(on)4 | $I_S = 5.15\text{ A}$, $V_{GS} = 3.1\text{ V}$ | 2.10 | 3.40 | 4.90 | |
| | RSS(on)5 | $I_S = 5.15\text{ A}$, $V_{GS} = 2.5\text{ V}$ | 2.20 | 3.50 | 6.70 | |
| | RSS(on)6 | $I_S = 5.15\text{ A}$, $V_{GS} = 2.25\text{ V}$ | 2.30 | 3.90 | 8.65 | |
| Body Diode Forward Voltage | $V_{F(s-s)}$ | $I_F = 5.15\text{ A}$, $V_{GS} = 0\text{ V}$ | | 0.7 | 1.0 | V |
| Input Capacitance ^{*1} | C_{iss} | $V_{SS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ kHz}$ | | 3500 | | pF |
| Output Capacitance ^{*1} | C_{oss} | | | 520 | | |
| Reverse Transfer Capacitance ^{*1} | C_{rss} | | | 450 | | |
| Turn-on Delay Time ^{*1, *2} | $t_{d(on)}$ | $V_{DD} = 6\text{ V}$, $V_{GS} = 0\text{ to }4\text{ V}$ | | 1.1 | | μs |
| Rise Time ^{*1, *2} | t_r | $I_S = 5.15\text{ A}$ | | 1.9 | | |
| Turn-off Delay Time ^{*1, *2} | $t_{d(off)}$ | $V_{DD} = 6\text{ V}$, $V_{GS} = 4\text{ to }0\text{ V}$ | | 4.8 | | μs |
| Fall Time ^{*1, *2} | t_f | $I_S = 5.15\text{ A}$ | | 3.0 | | |
| Total Gate Charge ^{*1} | Q_g | $V_{DD} = 6\text{ V}$ | | 29 | | nC |
| Gate-source Charge ^{*1} | Q_{gs} | $V_{GS} = 0\text{ to }4\text{ V}$ | | 7.9 | | |
| Gate-drain Charge ^{*1} | Q_{gd} | $I_S = 10.3\text{ A}$ | | 5.4 | | |
| Gate Resistance ^{*1} | R_g | $f = 1\text{ MHz}$ | 400 | 700 | 1000 | Ω |

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

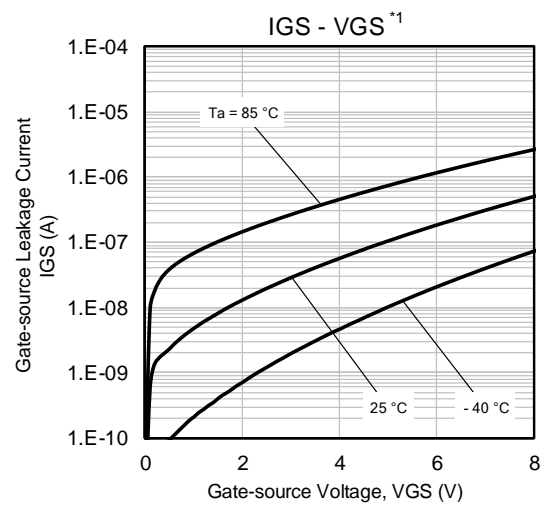
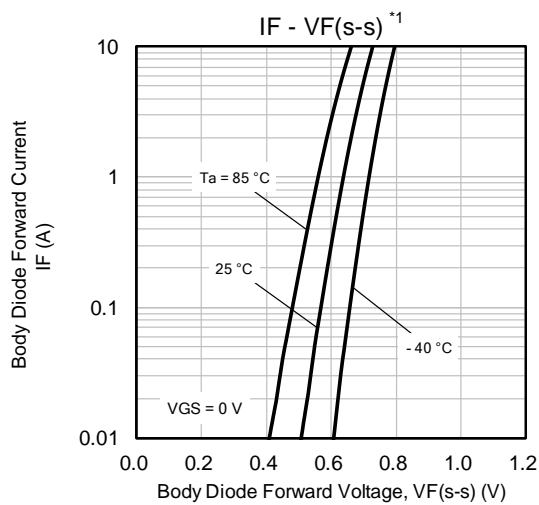
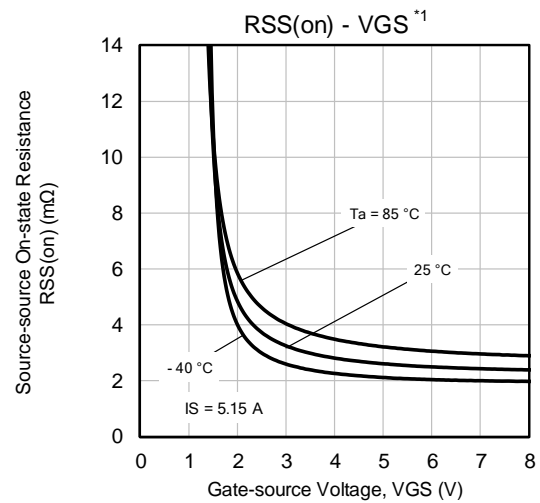
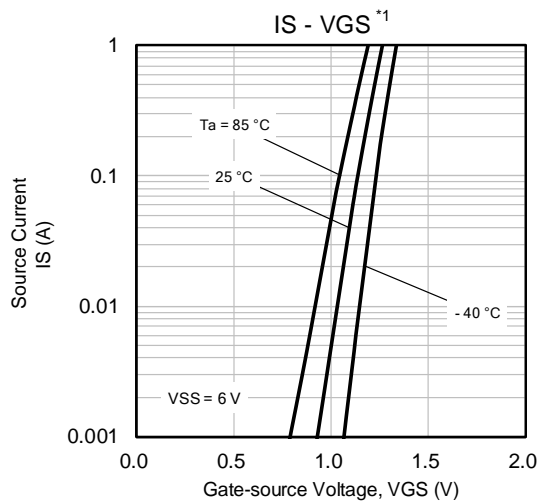
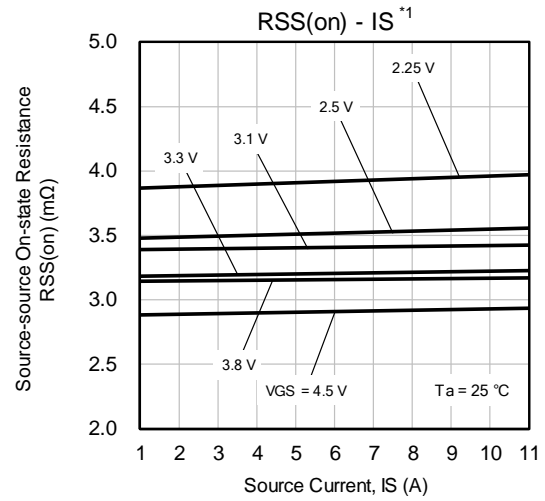
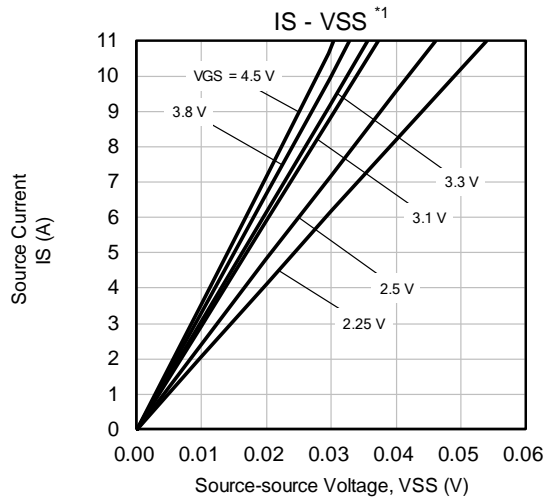
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.



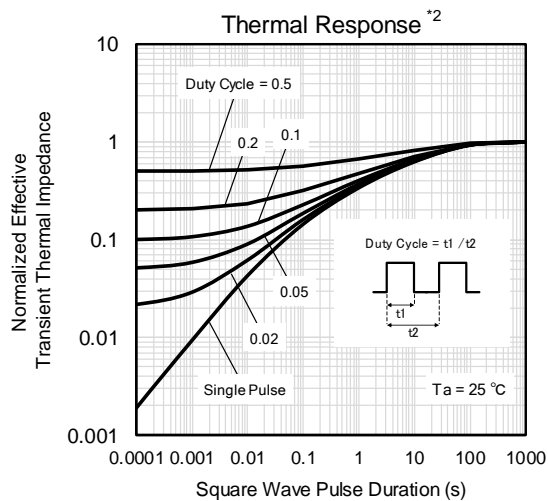
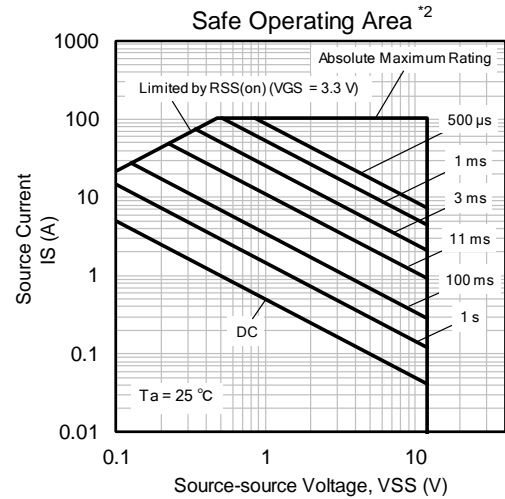
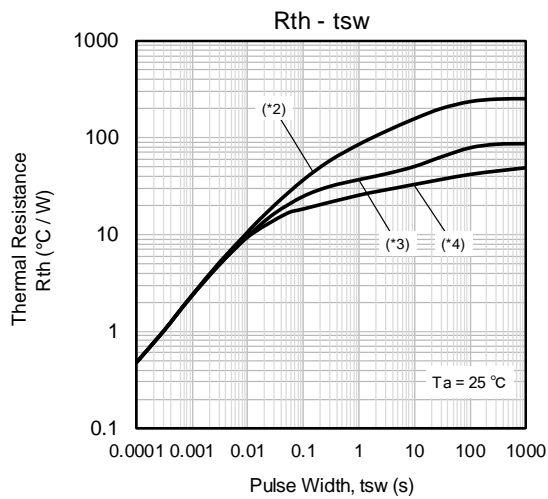
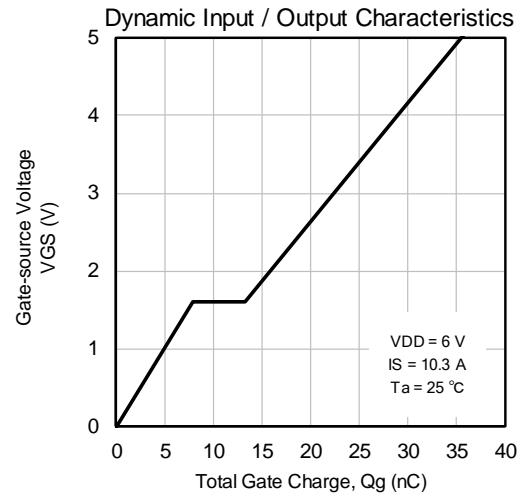
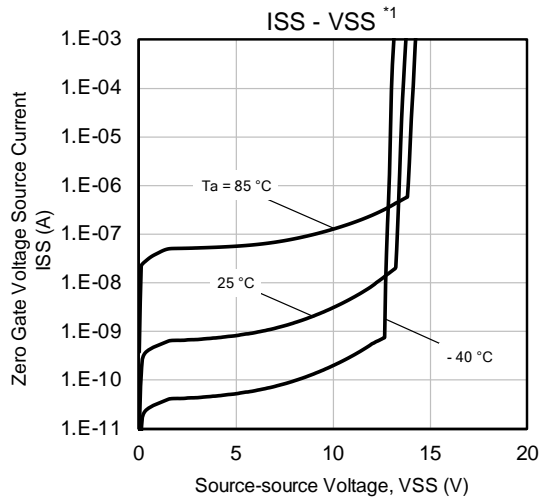
8. ELECTROSTATIC DISCHARGE CHARACTERISTIC $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

| Standard | Test Type | Symbol | Conditions | Class | Value | Unit |
|--------------|------------------|--------|--|-------|-----------------|------|
| AEC-Q101-001 | Human Body Model | HBM | $C = 100\text{ pF}$, $R = 1.5\text{ k}\Omega$ | H2 | > 2 to ≤ 4 | kV |

9. TECHNICAL DATA (Reference)



TECHNICAL DATA (Reference)



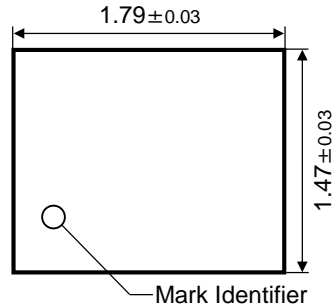
Note

- *1 Pulse measurement.
- *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
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(23 mm² area, 36 μm thickness).
- *3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
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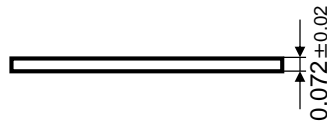
10. OUTLINE

(Top View)

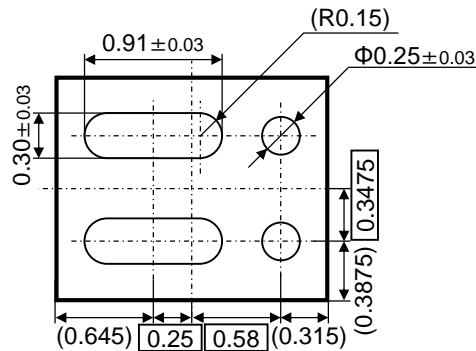
Unit: mm



(Front View)

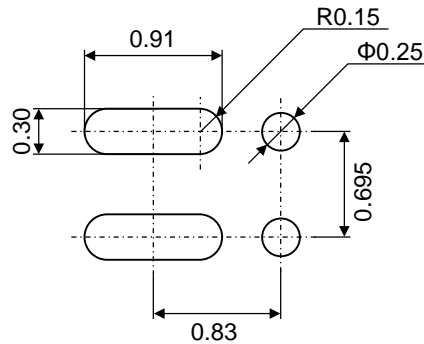


(Bottom View)



11. LAND & STENCIL PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

12. REVISION HISTORY

| Date | Revision | Description |
|-----------|----------|---|
| 2021.8.3 | 1.00 | 1. Initially issued. |
| 2021.12.1 | 2.00 | 1. Changed document name from Product Standards to Datasheet. |
| | | 2. Added MARKING SYMBOL. |
| | | 3. Added RSS(on) characteristics of condition VGS = 3.3 V & VGS = 2.25 V. |
| | | 4. Added package code. |
| | | 5. Added important notice in Land Pattern. |
| | | 6. Added special attention and precautions notes. |
| | | |
| | | |

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